MSR820 - Bandwidth Engine® 2 - Macro

Fast, Intelligent Data Access

PRODUCT BRIEF

RECORD PROCESSING OFFLOAD ENGINE

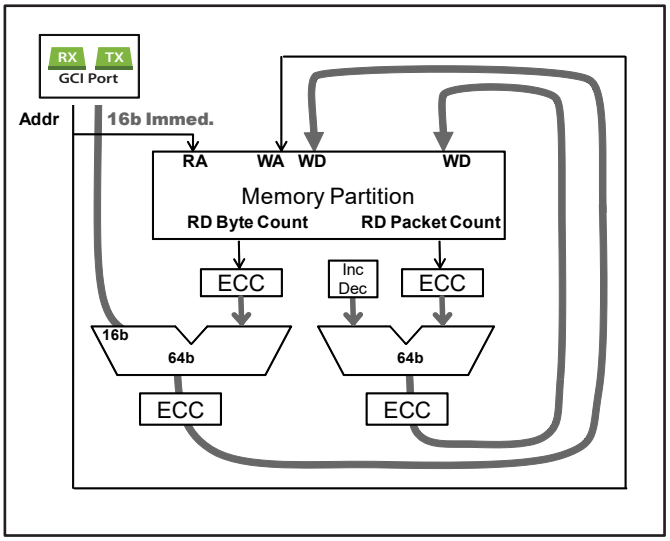
MoSys® Bandwidth Engine MSR820 adds on-board intelligence to the burst abilities of the MSR620, providing intelligent offload for Counting, Statistics, Metering and Atomic operations. The highly parallel array architecture can be saturated with only 8 SerDes lanes when utilizing the on-board macro functionality. Coupled with the efficient, packetized, serial interface, it enables support of multiple applications within the 576Mbit footprint.

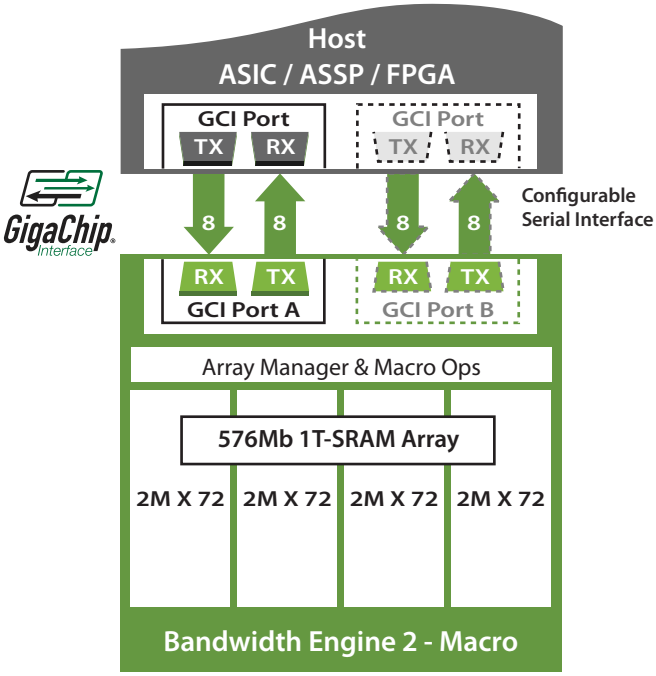
FIXED MACRO OPERATIONS

The macro pipelines include feed forward capabilities to combine back to back instructions to the same record, guaranteeing accurate accounting and relieving the host of this task.

- On-board Macro for 400G (600Mpps) Networks
  - 8M Single or Dual 64b 'lifetime' counters
  - 16M Dual-Split counters
  - 4M Flows - Two Rate Three Color Meter (trTCM)
  - 4M Flows - Single Rate Three Color Meter (srTCM)
- True Atomic Operations
- Burst to 400 Gbps Throughput
- Write broadcast two or four copies

INTERNAL PIPELINE DIAGRAM





ARCHITECTURAL INNOVATION

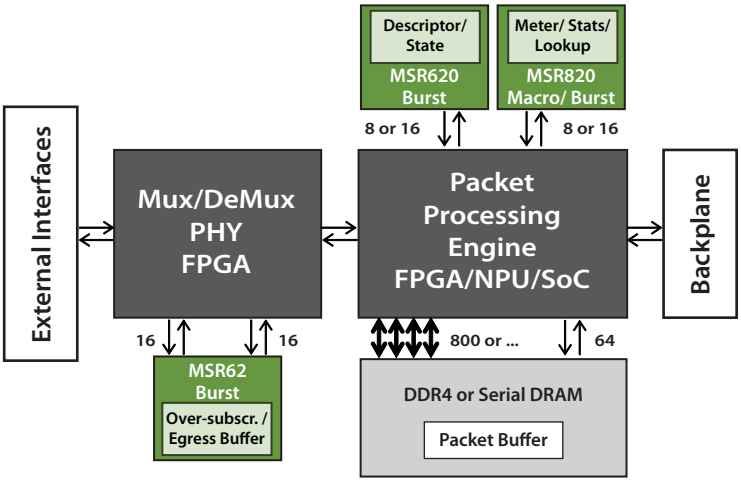
The Bandwidth Engine architecture elieviates memory access bottlenecks in data processing applications using a highly efficient serial interface and a highly parallel memory array. The intelligence and error resilience in the Array Manager, and reliable transport interface removes complexity from the host device and ensures end-to-end data integrity. The result is higher performance with fewer pins, less board area and improved economics versus traditional memory alternatives The Bandwidth Engine family was designed and built to ensure device reliability and data integrity.

FEATURES

- 576Mb 1T-SRAM® memory array architecture
  - 3 ns core cycle time, < 16 ns read latency
- Low-latency SerDes technology up to 15.625 Gbps
  - 4, 8 or 16 serial transceivers (TX/RX)
  - OIF CEI-11G-SR and XFI compatible interface
  - Tuned for low-power transmission up to 20 cm
- High-performance GigaChip® Interface
  - High-efficiency format utilizing scrambling
  - CRC error detection and recovery mechanisms
- Intelligent Error Management and Bit Safe® Technology
- High reliability – 1T-SRAM soft error immunity

NETWORKING APPLICATIONS

The metering and counting functions of the MSR820 Bandwidth Engine 2 - Macro device are intended for use in Shaping, Traffic Conditioning, and Operations Administration and Management (OAM) for enterprise, metro and carrier class services. The high access rate is well suited for table lookups and the high throughput burst function for buffer applications.



CYCLE SELECTABLE OPERATIONS

The MSR820 functionality is selectable on a cycle by cycle basis, allowing the use of the device in unified memory applications and optimizing the access patterns accordingly. Metering and Counting can be interspersed with Table Lookup applications which use a single word access, and in the next cycle a burst, broadcast or atomic operation as needed.

The Write Broadcast capability enables storing the same data into 2 or 4 partitions in a single command. Through the use of table replication, the access rate can be increased two or more times, enabling a table lookup every 640 picoseconds.

PACKAGING

- 324 FCBGA, 19mm x19mm, 1.0mm ball pitch
- 0.9 V/1.0V, 1.5 V supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I^2C configuration port

GIGACHIP® INTERFACE INNOVATION

A key element of the performance and power efficiency of the Bandwidth Engine is the use of a highly efficient and optimized interface. A less efficient interface would require additional pins to achieve the same level of performance. The GigaChip Interface (GCI) is an open, serial transport protocol optimized for high-bandwidth, high-efficiency, high-reliability chip-to-chip communications.

GCI builds on compatible CEI-11 or XFI SerDes with an optimized set of data link, transaction layer and error management features. It achieves a small logic footprint and lower system cost than other serial protocols. GCI omits features that are not needed for point-to-point communication over short distances.

GCI includes an automatic error recovery mechanism through the use of a replay buffer to retransmit frames in the event of a CRC error. The corrupted frame and all subsequent frames are dropped and replayed to guarantee end-to-end data integrity at all times.

GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

Commands are defined as 36-bit half words and sent to the device in pairs within the 72-bit payload.

Data words are transferred using the full 72-bit payload

INTERFACE PERFORMANCE

Configuration	GCI Ports	Lanes/port		Max Performance ** Giga-Accesses/sec			Throughput (Gbps)	Marcro Ops.
		Rx	Tx	Read	Write	Comb.	Burst of 8	(GOP/sec)
2 port, 16 lane*	2	8	8	2.50	1.25	3.75	320	12
2 port, 8 lane	2	4	4	1.25	0.63	1.88	160	12
1 port, 8 lane	1	8	8	1.25	0.63	1.88	160	12
1 port, 4 lane	1	4	4	0.63	0.31	0.94	80	6

*default configuration
** 36b writes & 72b Reads

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