MSR620 - Bandwidth Engine® 2 - Burst

Fast, Intelligent Data Access

PRODUCT BRIEF

THROUGHPUT & ACCESS ENGINE

MoSys® Bandwidth Engine MSR620 brings fast, intelligent memory access to data processing chipsets. The MSR620 integrates high density memory, a high speed serial interface, 90% efficient transport protocol, and payload burst capabilities to break the access and throughput barriers in networking, security, compute, video and other high speed data processing applications.

BURST PERFORMANCE

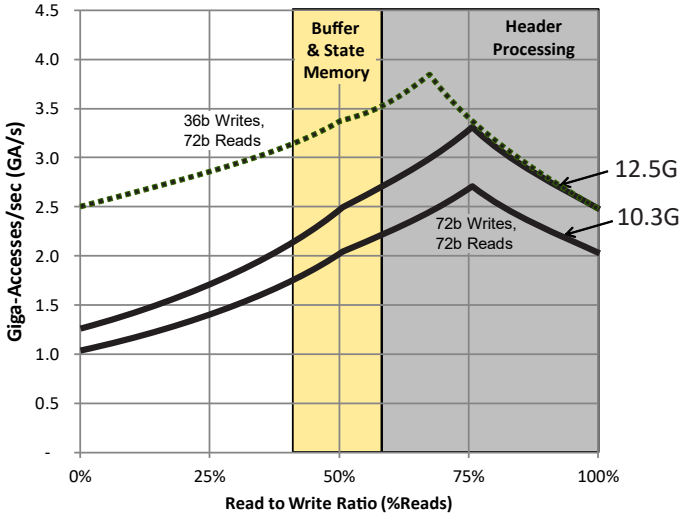
The burst functionality of the MSR620 provides up to 320 Gbps CRC-protected, data throughput. Burst length is selectable on a cycle by cycle basis for maximum flexibility.

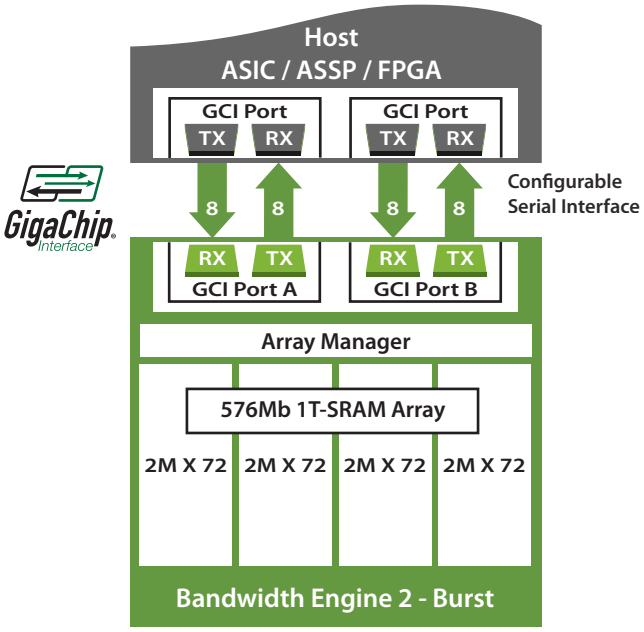
- Effective throughput of payload; 72b per word
- BL# = Burst Length; linear burst of 2, 4 or 8 words
- Full duplex: balanced read and write

Throughput (Gbps)		Speed Grade	
		-10	-12
Width	Burst	10.3125G	12.5G
16 lane	BL8	132.0	160.0
	BL4	118.8	144.0
	BL2	99.0	120.0
8 lane	BL8	66.0	80.0
	BL4	59.4	72.0
	BL2	49.5	60.0
4 lane	BL8	33.0	40.0
	BL4	29.7	36.0
	BL2	24.8	30.0

ACCESS PERFORMANCE

The device delivers over 3.3 billion 72-bit accesses per second.





ARCHITECTURAL INNOVATION

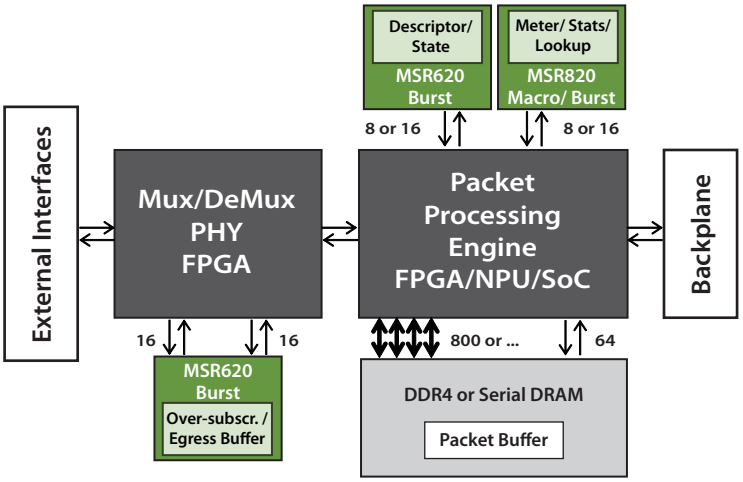
The Bandwidth Engine architecture elieviates memory access bottlenecks in data processing applications using a highly efficient serial interface and a highly parallel memory array. The intelligence and error resilience in the Array Manager, and reliable transport interface removes complexity from the host device and ensures end-to-end data integrity. The result is higher performance with fewer pins, less board area and improved economics versus traditional memory alternatives The Bandwidth Engine family was designed and built to ensure device reliability and data integrity.

FEATURES

- 576Mb 1T-SRAM® memory array architecture
  - 3 ns core cycle time, < 16 ns read latency
- Low-latency SerDes technology up to 12.5 Gbps
  - 4, 8 or 16 serial transceivers (TX/RX)
  - OIF CEI-11G-SR and XFI compatible interface
  - Tuned for low-power transmission up to 20 cm
- High-performance GigaChip™ Interface
  - High-efficiency format utilizing scrambling
  - CRC error detection and automatic recovery
- Intelligent Error Management and Bit Safe™ Technology
- High reliability – 1T-SRAM soft error immunity
- Advanced debugging capabilities

NETWORKING APPLICATION EXAMPLE

The MSR620 Bandwidth Engine 2 - Burst device is an optimal solution for high performance networking equipment with an aggregate bandwidth of 100G or higher. The burst feature of the MSR620 enables a single chip solution for 100G line rate buffering applications. The fast, intelligent access makes it suitable to accelerate packet lookup, descriptor or state applications as well.



CYCLE SELECTABLE BURST & WRITE BROADCAST

The MSR620 Burst functionality is selectable on a cycle by cycle basis, allowing the use of the device in unified memory applications and optimizing the access patterns accordingly. Table Lookup applications may use a high access burst of 1 and in the next cycle a buffer application could use a burst length optimized for the payload that needs to be buffered.

The Write Broadcast capability enables storing the same data into 2 or 4 partitions in a single command. Through the use of table replication, the access rate can be increased two or more times, enabling a table lookup every 640 picoseconds.

PACKAGING

- 324 FCBGA, 19mm x19mm, 1.0mm ball pitch
- 0.9 V/1.0V, 1.5 V supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I^2C configuration port

GIGACHIP™ INTERFACE INNOVATION

A key element of the performance and power efficiency of the Bandwidth Engine is the use of a highly efficient and optimized interface. An inefficient interface would require additional pins to achieve the same level of performance. The GigaChip Interface (GCI) is an open, serial transport protocol optimized for high-bandwidth, high-efficiency, high-reliability chip-to-chip communications.

GCI builds on compatible CEI-11 or XFI SerDes with an optimized set of data link, transaction layer and error management features. It achieves a small logic footprint and lower system cost than other serial protocols. GCI omits features that are not needed for point-to-point communication over short distances.

GCI includes an automatic error recovery mechanism through the use of a replay buffer to retransmit frames in the event of a CRC error. The corrupted frame and all subsequent frames are dropped and replayed to guarantee end-to-end data integrity at all times.

GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

Commands are defined as 36-bit half words and sent to the device in pairs within the 72-bit payload.

Data words are transferred using the full 72-bit payload

INTERFACE PERFORMANCE

Configuration	GCI Ports	Lanes/port		Max Performance** Giga-Accesses/sec			Throughput (Gbps)
		Rx	Tx	Read	Write	Comb.	Burst of 8
2 port, 16 lane*	2	8	8	2.50	1.25	3.75	320
2 port, 8 lane	2	4	4	1.25	0.63	1.88	160
1 port, 8 lane	1	8	8	1.25	0.63	1.88	160
1 port, 4 lane	1	4	4	0.63	0.31	0.94	80

*default configuration
** 36b writes & 72b Reads

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