MSRZ30 - Bandwidth Engine® 3
For EZchip NPS-400

PRODUCT BRIEF

MSRZ30 DESCRIPTION

The MoSys® MSRZ30 is a member of the Bandwidth Engine 3 family optimized for the EZchip NPS-400 network processor. It has 1152 Mb of 1T-SRAM® memory and on-board access scheduling.

The SerDes interface delivers full duplex, CRC protected data throughput and the memory array architecture is capable of up to three billion random memory reads per second.

BANDWIDTH ENGINE OVERVIEW

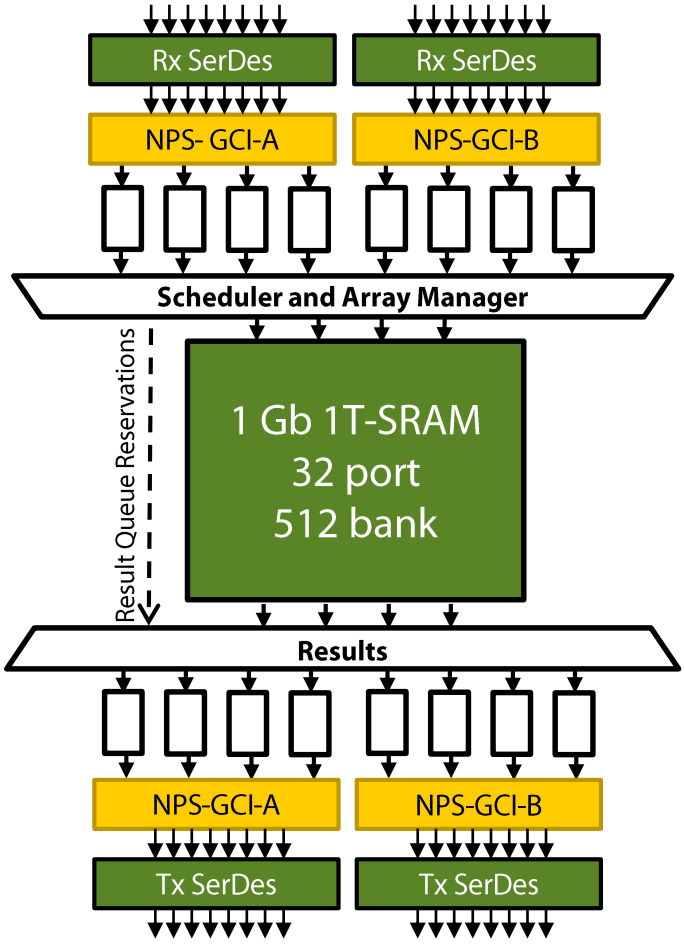
The Bandwidth Engine architecture is a highly parallel, multi-bank, multi-ported 1T-SRAM based memory array coupled with a high efficiency serial interface and on-board functionality, delivering intelligent scheduled access in addition to the highest memory transaction rate, table read rate and data throughput of any single chip device.

TRANSPARENT ACCELERATION

The MSRZ30 has been optimized for the NPS-400 network processor in terms of transfer size, efficiency and table structures. The addition of the MSRZ30 delivers a 50% increase in external memory bandwidth, which improves the packet process rate as well as the allowable complexity by providing more opportunity for table lookup within each packet arrival interval.

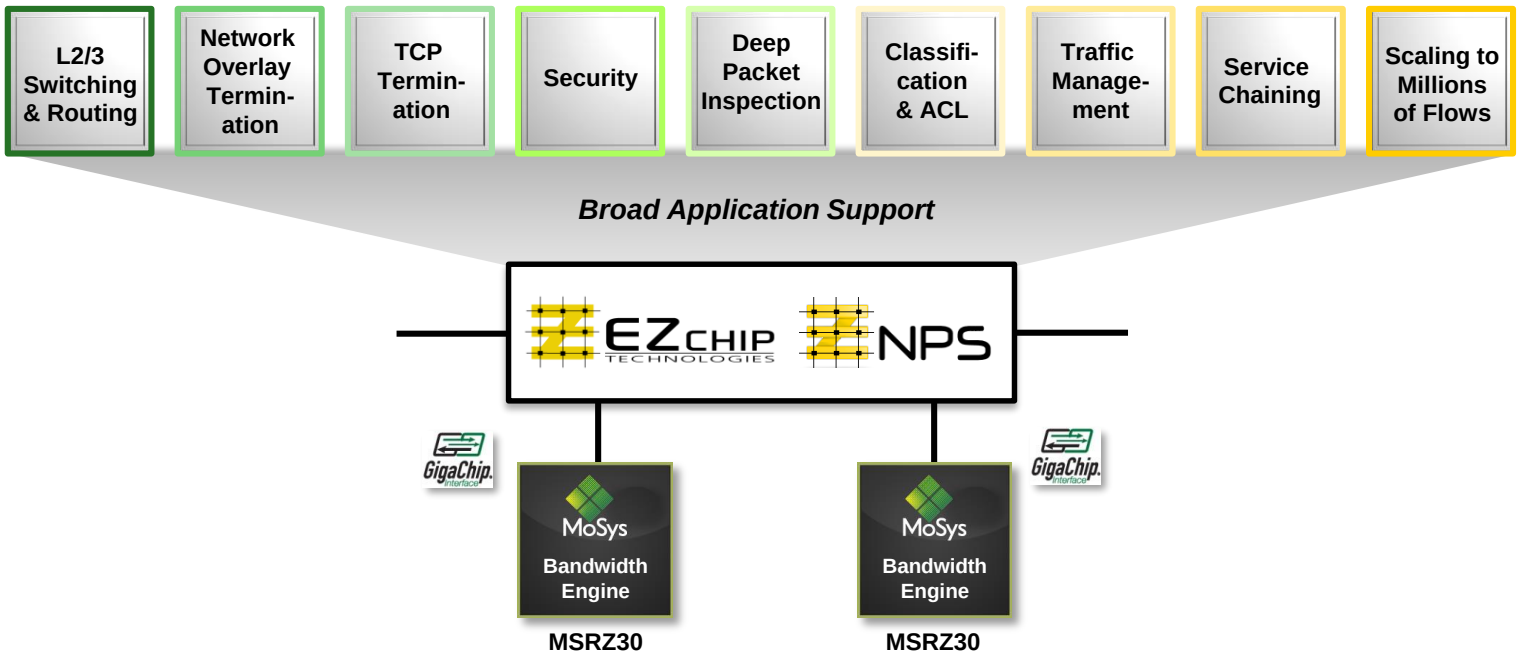
The NPS-400 allocates and manages the MSRZ30 resources without intervention from the user. Table and memory access is allocated transparently and dynamically between the DDR DRAM and the MSRZ30 based on the packet processing acceleration requirements. A single MSRZ30 is capable of supporting multiple applications and can also be shared between two host devices; each connecting to one GCI port, for greater capacity.

Datacenter and emerging high rate Software Defined Network (SDN) and Network Function Virtualization (NFV) can also take advantage of the acceleration and high access rate table lookups for flow based and application aware switching and routing.



FEATURES

- 1152Mb 1T-SRAM® memory array architecture
  - 3.2 ns core cycle time
- Up to three billion random reads per second
- Low-latency SerDes technology
  - 8 or 16 serial transceivers (TX/RX)
  - OIF CEI-11G-SR compatible
  - Tuned for low-power transmission up to 20 cm
- Open GigaChip® Interface delivers bandwidth, efficiency and reliability
  - Low latency protocol
  - Reliability with scrambling, CRC and error recovery mechanisms
- Intelligent Error Management & Bit Safe® Technology
- High reliability – 1T-SRAM soft error immunity
- Advanced debugging and evaluation capabilities with MoSys IC Spotlight software



UNIFIED MEMORY IMPLEMENTATIONS

The MSRZ30 functionality is selectable on a cycle-by-cycle basis with the large memory capacity and high speed allowing the use of the device in unified memory applications. Multiple tables and buffers can be defined with access interspersed between applications which could use each access command as needed.

BOARD DESIGN ATTRIBUTES

- 676 FCBGA, 27mm x 27mm, 1.0mm ball pitch
- 0.9V/1.0V, 1.5V, (1.8V EEPROM) supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I2C configuration port

ORDERING INFORMATION

Base Part Number	Temperature	Speed
MSRZ30AA	C	-15
	E	-12

GIGACHIP INTERFACE

The GigaChip Interface (GCI) is an open, freely licensable, efficient transport layer built on compatible, industry standard SerDes. GCI is optimized for small packet, chip-to-chip communications including error detection and recovery mechanisms.

GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

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